UNIVERSITY QUESTION BANK
DSP PROCESSOR & ARCHITECHTURE

Unit I

SUMMER - 16

Q1. Distinguish between single Access RAM and double Access RAM used in on-chip memory of TMS320CSX processor. Explain how memory access is increased in programmable DSPs? (7)
Q2. Explain what is meant by instruction pipelining? A non-pipelined system takes 100ns to process a task. The same task can be performed in 4 segments pipelined into 20ns each. Determine speedup ratio of pipeline for 1000 tasks. (7)
Q3. Draw basic block diagram of MAC unit used in PDSPs. Explain how it is used to perform convolution. (6)
Q4. Describe the circular addressing mode with example. (4)
Q5. What is range of numbers that can be represented in a fixed point format using 16 bits, if the numbers are treated as? i) Signed integers ii) Signed fractions (4)

WINTER – 16

Q1. Explain the difference between Von-Neumann and modified Harvard Architecture. (7)
Q2. Explain what is meant by Instruction pipelining? A non-pipelined system takes 80ns to process a task. The same task can be performed in 4 segments pipelined into 20ns each. Determine speedup ratio of pipeline for 1000 tasks. (7)
Q3. Draw basic block diagram of MAC unit used in PDSPs? Explain how it is used to perform convolution. (7)
Q4. Distinguish between multiple access memory and multi ported memory. (7)

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Q1. Draw basic block diagram of MAC unit and explain how convolution is performed using a single MAC unit. (7)
Q2. A non pipelined system takes 100 nsec to process a task. The same task can be performed in 5 segments pipelined into 10 nsec each. Determine speed up ratio of pipeline for 1000 tasks. (6)
Q3. Explain the difference between Von Neumann and Harvard architecture for the processor. Which architecture is preferred for DSP applications and why? What is modified Harvard Architecture? (7)
Q4. A DSP has a circular buffer with the start and the end addresses as 0210 h and 0201 h respectively. What would be the new value of the address pointer of the buffer if in the course of address computations, it gets updated to a) 0212 h b) 01FC h. (6)

WINTER – 17

Q1. Explain the difference between Von-Neumann and Harvard architecture for the computer. Which architecture is preferred for DSP applications and why? (7)
Q2. Define the following terms: i) Multiple access memory. ii) Multi ported memory. (4)
Q3. Explain why MAC operation is implemented in hardware in programmable DSPs. (2)
Q4. Explain what is meant by instruction pipelining. Explain with an example how pipelining increases the throughput efficiency. (8)
Q5. What is range of numbers that can be represented in a fixed point format using 16 bits, If the numbers are treated as a) Signed integers b) Signed fractions (5)

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Q1. Explain what is meant by instruction pipelining? A non-pipelined system takes 100 nsec to process a task the same task can be performed in 4 segments pipelined into 20 nsec each. Determine speed up ratio of pipeline for 1000 tasks. (8)

Q2. What is range of numbers that can be represented in a fixed point format using 16 bits, if the numbers are treated as a) Signed Integers b) Signed fractions (5)

Q3. Explain how a higher throughput is obtained using VLIW architecture. Give an example of DSP that has VLIW architecture. (7)

Q4. A DSP has a circular buffer with the start and the end addresses as 0210 h and 0201 h, respectively. What would be the new values of the address painter of the buffer if in the course of address computation, it gets updated to a) 0212 h b) 01 fc h (6)

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Q1. Elaborate how pipelined architecture in DSP processors have improved its performance. (7)

Q2. Discuss the convolution operation in DSPs using MAC unit. (6)

Q3. Illustrate the circular mode of addressing in DSP with example. (5)

Q4. Justify for a TMS 320 C5X processor the memory access procedure is consisting of onchip RAM memory access. (8)

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Q1. Explain the difference between von-Neumann and Harvard architecture for the computer. Which architecture is preferred for DSP application and why? (7)

Q2. Explain what is meant by instruction pipelining? A non-pipelined system takes 100ns to process a task. The same task can be performed in 4 segments pipelined into 20ns each. Determine speed up ratio of pipeline for 1000 tasks. (6)

Q3. Draw basic block diagram of MAC unit and explain how convolution is performed using a single MAC unit? (7)

Q4. Distinguish between multiple access memory and multiported memory. (6)

Unit II

SUMMER – 16

Q1. What is status register? List bits of STO of 5X and their functions. (4)

Q2. Explain direct addressing mode of C5X. Explain execution of instruction ADDC 20h with address generation process if content of DP=06 h and content of data memory location 0320h to 032f h are 20h. Take content of ACC as 30 h. (9)

Q3. Explain bus structure of TMS320C5X PDSP. (7)

Q4. Let the content of ARP, AR2 and INDX register be 2, 1250 h and 2 h respectively and contents of data memory location 1240 h-1260 h be filled with the data 2345 h. Let SXM be 0. Find the value of ACC and AR2 after sequential execution of following instructions.

i) LACC *, 0 ii) LACC*+,1 iii) LACC * -,3 (6)

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Q1. Explain the Architecture of DSP TMS320C5X. (6)

Q2. Explain the status register STO of TMS320C5X in detail. (7)

Q3. Explain the addressing modes of TMS320C5X. (6)

Q4. Explain the statue register ST1 of TMS320C5X in detail. (7)

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Q1. Draw the internal architecture diagram of 5X and indicate the various blocks. (8)

Q2. Let the content of ARP. AR_2 be 2, 1250 h respectively and contents data memory location 1240 h – 1260 h be filled with the data 2345 h. Let 5XM be 0. Find the value of ACC, AR2, ARP after execution of ADD *, 2 instructions. (6)

Q3. What is status register? List bits of ST0 and ST1 of 5X and their functions. (8)

Q4. Let the content of ARP, AR2 and INDX register be 2, 1250 h and 2 h respectively and contents of data memory location 1240 h – 1260 h be filled with the data 2345 h. Let 5XM be 0. Find the value of ACC and AR2 after execution of following instructions. 1) LACC *, 0 2) LACC * 0+, 1 3) LACC * – , 2 (6)

WINTER – 17

Q1. What are the different buses of TMS320C5X and their functions? (5)

Q2. List the status register bits of 5X and their functions. (5)

Q3. What are features of a central arithmetic logic unit of TMS320C5X. (3)

Q4. Explain direct addressing mode and show with a diagram has 16 bit address is formed.(5)

Q5. Let the value of ARP, AR2 and INDX register be 2, 1250 h and 2h respectively and the content of the data memory location 1240h-1260h be filled with the data 2345h. Let SXM be 0. The value of ACC and AR2 after the following sequence of LACC (Load accumulator with shift) instructions are executed serially. (8)

LACC *, 0
LACC * +, 1
LACC *-, 2
LACC *0 +, 4
LACC *0-, 3

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Q1. Draw block diagram of TMS320C5X architecture & explain. (8)

Q2. Explain the following instruction

LMMR ARO, 1500 h
SMMR ARO, 1500 h

Contents of ARO and data memory location 1500 h are 2345 h and 6789 h respectively. What are the results after execution of above instructions? (6)

Q3. Explain direct addressing mode of C5X. Explain execution of instruction ADDC 16 h with address generation process if content of DP = 06 h & content of Data Memory location 0320 h to 032 f h are 20 h. Take content of ACC as 30 h. (6)

Q4. What is status register? List bits of ST0 and ST1 of 5X and their functions. (8)

WINTER – 18

Q1. Elaborate the TMS 320 CXX architecture. (8)

Q2. Explain the operations performed when the TMS 320 C5X issues the following instructions;

i) ADD C 20 h
ii) SMMR ARO 1800 h
iii) BLDP 00 h (6)

Q3. A attenuator is to be designed using a DSP processor TMS 320 C5X. Illustrate the design stages required, onchip peripherals used. Also draw a system block diagram. (10)

Q4. Explain the role of status registers in determining the acquication of real time signal.(5)

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Q1. Let the content of ARP, AR2 and INDX register be 2, 1250h and 2h respectively and contents of data memory location 1240h-1260h be filled with the data 2345h. Let SXM be 0. Find the value of ACC and AR2 after sequential execution of following instructions
i) LACC *, 0 ii) LACC * -, 1 iii) LACC * -, 3 (7)

Q2. Explain the status register STI of TMS320C5X in detail. (7)

Q3. Explain the architecture of DSP TMS320C5X (8)

Q4. Explain the status register STO of TMS320C5X in detail. (6)

Unit – III

SUMMER – 16

Q1. Explain any three of the following instructions. i) MACD ii) ADD *,1
iii) SUB#2345 h, 1 iv) BD PGM 1250 h (6)

Q2. Draw the table showing the content of the instruction pipeline when following program is executed. Explain.

```
ZAP
BD PGM 1250 h
ADD*
SACL*+
MAC 4500 h, 25 h
PGM1250 h: LACC *+
```

(7)

Q3. Draw block diagram of DSP starter kit C5XDSK. What are the addresses of the program memory address space and data memory address space in the DSP starter kit where user programs and data may be stored? (8)

Q4. Mention few applications of each of the families of TI DSPs. (5)

WINTER – 16

Q1. Write an assembly language program using instructions of TMS320C5X processors to multiply two numbers of unsigned 32 bit data. Assume that the two data are available in memory save the 64 bit product in memory. (10)

Q2. Describe the circular addressing mode with example. (3)

Q3. Draw block diagram of DSP starter kit C5X DSK. What are the addresses of the program memory address space and data memory address space in the DSP starter kit where user programs and data may be stored? (10)

Q4. Explain the Instructions. i) MACD ii) LACC * +, 0 iii) SACH (3)

SUMMER – 17

Q1. Explain following instructions. 1) SUB 55 h, 2 2) LST #1 3) MACD 4) MPY (8)

Q2. Draw the table showing the content of the instruction pipeline when following program is exerted. (5)

```
ZAP
BD PGM 1250 h
ADD
SACL+
MAC 4500 h, 25 h
PGM 1250 h : LACC+
```

Q3. Draw block diagram of DSP starter kit C5X DSK. What are the addresses of the program memory address space and data memory address space in the DSP starter kit where user programs and data may be stored? (7)

Q4. Mention few applications of each of the facilities of TI DSPs (6)

WINTER – 17

Q1. Explain the following instructions LST, LAR, ADD, SUB, LMMR. (10)

Q2. Write the contents of memory locations after execution of LST # 0, 00h. if DP = 8. Before execution (4)

Data Mem 400h	3E00h
ST0	5E00h
ST1	09A0h

Q3. Consider the following program involving only single word instructions:

```
ADD *+
SAMM TREG 0
MPY *+
SQRA *+, AR2
```

Show the table showing contents of instruction pipeline. (7)

Q4. Explain the block diagram of DSP starter kit. (7)

SUMMER - 18

Q1. Explain any three instructions i) ADD * + ii) LST #0 iii) BD . PGM 1250 h iv) BLDP 00h (6)

Q2. Consider the following program involving only single word single cycle instruction. Draw the table showing the content of the instructions pipeline.

```
ADD*+
SAMM TREGO
MPY *+
SQRA*+, AR2
```

(7)

Q3. Mention few application of each of the families of TI DSPs. (6)

Q4. Draw block diagram of DSP starter kit C5XDSK and explain. (7)

WINTER – 18

Q1. An image processing application needs to be designed using a DSP processor based starter kit with C5X. The image to be acquired has only two color tones i. e. black & grey. The images are of the size 50x50 pixcels. The real time signal to be processed should be acquired using which configuration. Also write a sample ALP for the same. (13)

Q2. Discuss the various functions available in C5X DSK starter kit. (6)

Q3. Explain how multiplication operation can be performed on TI DSP family of processors.(7)

SUMMER – 19

Q1. Explain the following instructions LST, LAR, ADD, SUB, LMMR. (8)

Q2. Write the contents of memory locations after execution of LST # 0, 00h. if DP = 8. Before execution (5)

Data Mem 400h	3E00h
ST0	5E00h
ST1	09A0h

Q3. Explain following instructions 1) SUB 8Sh, 2 2) LACC * + , 0 3) MACD 4)MPY (8)

Q4. Write the content of accumulator after execution of LACC *, 4 if SXM = 0 of fig. (b)

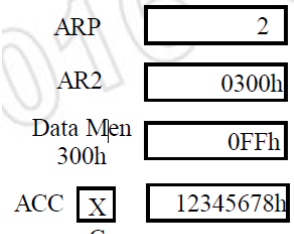

Fig. (b)

Unit – IV

SUMMER – 16

Q1. Explain data addressing modes of TMS320C54X processor. (8)

Q2. Explain program control unit of TMS320C54X. (5)

Q3. Explain how interrupts are handled in TMS320C54X P DS P? (6)

Q4. Draw and explain central processing unit of C54X in detail. (7)

WINTER – 16

Q1. Explain the Architecture of TMS320C54X in detail. (7)

Q2. Explain the following instructions i) LST ii) SAMM ii) SAR iv) SACC v) LACC vi) LDP (6)

Q3. Explain data addressing modes of TMS320C54X processor. (6)

Q4. Explain how interrupts are handled in TMS320C54X PDSP. (7)

SUMMER – 17

Q1. Explain internal memory organization of C54X. (6)

Q2. How many buses are there in C54X. Explain each in detail. (7)

Q3. Explain phases of pipelining of TMS320C54X processor. (7)

Q4. Explain following data addressing modes of TMS320C54X processor. 1) Absolute 2) Accumulator 3) Stack (6)

WINTER – 17

Q1. Draw the block diagram of TMS320C54X and explain the following blocks. (Describe in brief the following blo)
i) Arithmetic and logic unit ii) Accumulators iii) Barrel shifter iv) CSSu
v) Address generation unit in brief. (10)

Q2. Explain TDM serial port with respect to TMS320C54X. (3)

Q3. Describe stack, accumulator and absolute addressing mode with respect to TMS320C54X. (6)

Q4. Write in brief about interrupts handling in TMS320C54XX. (7)

SUMMER – 18

Q1. Draw complete architecture of TMS320C54X and explain in brief. (7)
Q2. Write note on instruction pipelining of TMS320C54X processors. (6)
Q3. How interrupts are handled in TMS320C54X processor. Explain with flow chart. (7)
Q4. Explain following addressing modes in TMS320C54X processor.
1) Absolute 2) Stack 3) Accumulator (6)

WINTER – 18

Q1. Write a short note on interrupts of TMS 320 C54 XX & how they are handled. (7)
Q2. How the program control works when the TMS 320 C54XX is executing a instruction in data addressing mode. (6)
Q3. Explain the bus architecture of TMS 320 C54XX. (6)
Q4. Illustrate the role of onchip peripherals in a signal processing application. (7)

SUMMER – 19

Q1. Draw and Explain central processing unit of C54X in detail. (7)
Q2. How many buses are there in C54X. Explain each in detail. (6)
Q3. How Interrupts are handled in TMS320 C54X processor. Explain with flow chart. (7)
Q4. Explain following data addressing modes of C54X processor. 1) Absolute
2) Accumulator 3) Stack (6)

Unit – V

SUMMER – 16

Q1. List the features of TMS320C6X processor. (7)
Q2. Give the brief introduction of Motorola DSP563XX processor. (7)
Q3. Compare the features of C5X, C54X, and C6X in detail. (8)
Q4. Write steps for creating new project and building Assembly language code in CCS. (6)

WINTER – 16

Q1. Compare the features of C5X, C54X and C6X in detail. (7)
Q2. Explain the Architecture of Motorola DSP 563XX. (6)
Q3. Write steps for creating new project and building Assembly language code in CCS. (6)
Q4. Draw and explain the architecture of TMS320C6X. (7)

SUMMER – 17

Q1. List the features of TMS320C6X processor. (7)
Q2. Write a short note on Code Composer Studio (CCS). (6)
Q3. Compare the features of C5X, C5AX and C6X in detail. (7)
Q4. Give the brief introduction of Motorola DSP563XX processor. (6)

WINTER – 17

Q1. Draw the architecture of TMS320C6X and explain the working of central processing unit and data paths. (8)
Q2. What is code composer studio? How to build project in CCS. (5)
Q3. Compare the features of DSP processors TMS320C5X, TMS320C54X, TMS320C6X. (6)
Q4. Draw an architecture of Motorola DSP563XX and explain in brief. (7)

SUMMER – 18

Q1. List the features of TMS320C6X processor. (7)
Q2. Write steps for creating new project and building assembly language code in CCS. (6)
Q3. Give the brief Introduction of Motorola 563XX processor. (7)
Q4. Compare the features of TMS320C5X and TMS320C54X processor. (6)

WINTER – 18

Q1. Elaborate the cross platform Development process in TMS 320 C6X. (4)
Q2. Discuss the architecture of Motorola DSP 563XX Explain how its is advantageous over TI DSP's. (9)
Q3. Explain the firmware development process in DSP processors. (7)
Q4. List the comparison of the features of DSP family of processors like TMS 320 C6X & TMS320 C5X. (6)

SUMMER – 19

Q1. Compare the features of DSP processors C5X, C54X, C6X. (7)
Q2. Write steps of creating new project and building Assembly language code in CCS. (7)
Q3. Give the brief introduction of Motorola DSP563XX processor. (7)
Q4. Draw the architecture of C6X and explain the working of central processing unit and data paths. (7)

Unit – VI

SUMMER – 16

Q1. Explain filtering of long data sequence using overlap save method. (3)
Q2. Find the output y (n) of a filter whose impulse response is h (n) = {9, 10} and input signal x (n) = {1, 2, 3, 4, 5, 6, 7, 8} Using overlap add method. (10)
Q3. Input sequence of 75 elements is to be convolved with an impulse response of a filter with 45 elements using FFT and IFFT. Determine total number of complex multiplications and additions needed to implement the convolution. The computation is to be implemented on a fixed point signal processor that takes 10 ns to do a real integer multiplication. Determine the computation time for complex multiplications involved. (8)
Q4. Explain digital decimation filter implementation for decimation factor = 2 using 3-tap FIR filter. (5)

WINTER – 16

Q1. Input sequence of 75 elements is to be convolved with an impulse response of a filter with 45 elements using FFT and IFFT. Determine total number of complex multiplications and additions needed to implement the convolution. The computation is to be implemented on affixed point signal processor that takes lons to do a real integer multiplication. Determine the computation time for complex multiplications involved. (8)
Q2. Explain wavelet transform and compare with Fourier transform. (6)
Q3. Perform linear convolution of the following sequences by
(a) overlap Add method and
(b) overlap save method.
x(n) = {1, -1, 2, -2, 3, -3, 4, -4}; h(n) = {-1, 1} (8)
Q4. Explain the time complexity of DFT and FFT algorithm. (6)

SUMMER – 17

Q1. Write short note on interpolation filter. (6)

Q2. Find the output y (n) of a filter whose impulse response is h(n)={9, 10} and input signal x(n)={1, 2, 3, 4, 5, 6, 7, 8} using overlap save method. (8)

Q3. Input sequence of +5 elements is to be convolved with an impulse response of a filter with 45 elements using FFT and IFFT. Determine total number of complex multiplications and additions needed to implement the convolution. The computation is to be implemented on a fixed point signal processor that takes 10 ns to do a real integer multiplication. Determine the computation time for complex multiplication involved.(8)

Q4. Explain wavelet filter. (6)

WINTER – 17

Q1. Describe overlap same and overlap add methods for filtering long data sequences. (8)

Q2. A time domain sequence of 73 elements is to convolved with another time domain sequence of 50 elements using DFT to transform the two sequences, multiplying them and taking IDFT to obtain resulting time domain sequence. DIT algorithm is used to take DFT and IDFT. Determine the total number of complex multiplications needed to implement the convolution. Assume that each butterfly computation requires one complex multiplication. (6)

Q3. Write short notes on **any three.** (14)

1) Interpolation filter
2) Decimation filter
3) Wavelet filter
4) Comparison of DFT and FFT time complexity.

SUMMER – 18

Q1. Explain filtering of long data sequence using overlapp save method. (7)

Q2. Find the output y(n) of a filter whose impulse response is

h (n) ={1,1,1}and input signal

x (n) = {3,-1,0,1,3,2,0,1,2,1} using overlap add method. (7)

Q3. Explain the following **any two.**

i) Wavelet filter. ii) Decimation filter with decimation factor = 3 using 5 tap FIR filter. iii) Interpolation filter. (10)

Q4. A time domain sequence of 73 elements is to be convolved with another time domain sequence of 50 elements using FFT & IFFT. Determine total number of complex multiplications & additions needed to implement the convolution. (4)

WINTER – 18

Q1. Write short notes on **any two**. (7)

1) Up sampling
2) Down sampling
3) DFT block used in TI DSP

Q2. Explain how filtering of long data sequence is done. (7)

Q3. A time domain sequence of 80 elements is to be convolued with another sequence of 100 elements using FFT & IFFT operations. Determine the total number of complex multiplications & additions required. (5)

Q4. Elaborate digital decimation filter implementation for decimation factor = 3 using 3 tap FIR filter. Also realize the final FIR filter using delay elements. Summing points & multipliers. (9)

SUMMER – 19

Q1. Explain filtering of long data sequence using overlap and save method. (3)

Q2. Find the output y(n) of a filter whose impulse response is h(n) = {9 10} and input signal x (n) = {1 2 3 4 5 6 7 8} using overlap and add method. (10)

Q3. Write short notes on **any three**. (13)

a) Interpolation filter
b) Decimation filter
c) Wavelet filter
d) Comparison of DFT and FFT time complexity.